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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,200	08/29/2001	Eugene P. Marsh	150.0064 0102	8194

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EXAMINER	
NGUYEN, JOSEPH H	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	09/942,200	MARSH, EUGENE P.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-39 and 41-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-39 and 41-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/9/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 23, 26-28, 30-35, 37-38, 42, 44-45 and 47 are rejected under 35 U.S.C. 102(b) as being anticipated by Wolters et al. (US 5,744,832, hereinafter, "Wolters").

Regarding claim 23, Wolters discloses on figure 6 a semiconductor device structure comprising a substrate assembly 3 (col. 4, line 59) including a surface; and a barrier 111 over at least a portion of the surface, wherein the barrier layer 111 is formed of a platinum(x): ruthenium alloy where x is in the range of about 0.60 to about 0.995 (col. 7, lines 13-14). Wolters teaches in col.7, lines 13-14 that layer 111 contains platinum and ruthenium wherein the atomic percent of ruthenium is approximately 15%-20% (0.15-0.20), which means the value of x (atomic percent of platinum) is approximately 0.80-0.85, which falls in the claimed range of 0.60 -0.995. Further, the term "chemical vapor deposited" is merely product by process and therefore does not structurally distinguish from Wolters et al. herein.

Regarding claim 26, Wolters discloses on figure 6 the portion of the surface is a silicon-containing surface (col. 7, line 41-41).

Regarding claim 27, Wolters discloses on figure 6 a capacitor structure comprising a first electrode 11 (col. 4. line 62); a dielectric material 12 (col. 4,line 63) on at least a portion of the first electrode; and a second electrode 12 (col. 4, line 63) on the dielectric material, wherein the first electrode 11 comprises a barrier 111 layer of platinum (x): ruthenium alloy (col. 7, lines 13-14).

Regarding claim 28, Wolters discloses that x is in the range of about 0.60 to about 0.995(col. 7, lines 13-14).

Regarding claim 30, Wolters discloses on figure 6 are least one of the first electrode and second electrode comprises the barrier layer 111 of platinum (x): ruthenium alloy (col. 7, lines 13-14), and one additional conductive layer 110 (col. 7, lines 12-13).

Regarding claim 31, Wolters discloses the one additional conductive layer 110 is formed from material selected from the group of metal alloy (col. 7, lines 12-13).

Regarding claim 32, Wolters discloses on figure 6 a memory cell structure comprising a substrate 3 including at least one active device 1 (col. 4, line 60); and a capacitor 2 (col. 4, line 61) formed relative to the at least one active device, the capacitor comprising at least one electrode 11 including a barrier layer 111 formed of platinum (x): ruthenium alloy (col. 7, lines 13-14).

Regarding claim 33, Wolters discloses on figure 6 the capacitor includes a first electrode 11 formed relative to a silicon containing region 5 (col. 7, lines 39-41) of the at least one active device 1; a dielectric material 12 (col. 4, line 63) on at least a portion of the first electrode; and a second electrode 13 on the dielectric material, wherein the first

electrode 11 comprises the barrier layer 111 formed of platinum (x): ruthenium alloy (col. 7, lines 13-14).

Regarding claim 34, Wolters discloses on figure 6 the first electrode 11 comprising the barrier layer 11 formed of platinum (x): ruthenium alloy which includes one additional conductive layer 110 (col. 7, lines 12-13).

Regarding claim 35, Wolters discloses that x is in the range of about 0.60 to about 0.995 (col. 7, lines 13-14).

Regarding claim 37, Wolters discloses on figure 6 an integrated circuit structure comprising a substrate 3 assembly including at least one active device 1; and an interconnect 2 formed relative to the at least one active device, the interconnect including a barrier layer 111 formed of platinum (x): ruthenium alloy.

Regarding claim 38, Wolters discloses that x is in the range of about 0.60 to about 0.995 (col. 7, lines 13-14).

Regarding claim 42, Wolters teaches in col. 6, lines 6-12 that a layer of 200 nm (2000A) platinum/ruthenium is provided on the surface of the semiconductor body, and this layer is sputtered and eventually sputtering process will deposit alternatively a ruthenium and a platinum layer of approximately 1 to 1.5 nm (10-15A). Therefore, Wolters teaches that a thickness of the barrier layer is in a range of about 10A to about 10,000A.

Regarding claim 44, Wolters discloses on figure 6 the substrate assembly 3 comprises at least one active device 1 (col. 4, line 60).

Regarding claim 45, the term "chemical vapor deposited" is merely product by process. Therefore, a chemical vapor deposited barrier layer does not structurally distinguish from the barrier layer 111 of Wolters.

Regarding claim 47, Wolters teaches that a thickness of the barrier layer is in a range of about 10A to about 10,000A (col. 6, lines 6-12).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 41 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolters and further in view of Bronner et al. (US 6,177,696).

Regarding claims 41 and 46, Wolters discloses on figure 6 substantially all the structure set forth in the claimed invention except a substrate assembly comprising a small high aspect ration opening. Applicant teaches in page 14, lines 15-21 of the instant application that a small high aspect ratio opening is the one in which the width is less than about 1 micron and the depth is larger than the width. Bronner et al. teaches in col. 4, lines 30-45 that the opening (trench) 1 formed within a structure including a semiconductor substrate and that the opening has the depth of about 6 microns and the width of about 0.175 micron. Therefore, Bronner et al. teaches about the substrate comprising a small high aspect ratio opening. In view of such teaching, it would have

been obvious to one of ordinary skill in the art at the time the invention was made to modify Wolters by having a substrate assembly comprising a small high aspect ratio opening for the purpose of increasing the amount of charges stored per semiconductor substrate surface area (col. 1, lines 39-42, Bronner et al.).

Claims 43 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolters and further in view of Akram (US 2002/0056863 A1).

Regarding claims 43 and 48, Wolters discloses on figure 6 substantially all the structure set forth in the claimed invention except the thickness of the barrier layer being about 100A to about 500A. However, Akram teaches in para [0065], lines 13-14 that the thickness of the barrier layer 66 is about 10nm (100A) to about 500nm (5000A), which has its lower limit in the claimed range. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wolters by having the thickness of the barrier layer being about 100A to about 500A for the purpose of eliminating charge leakage (para [0015], line 5, Akram).

Claims 24, 25, 29, 36, 39 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolters.

Regarding claims 24, 29, 36 and 39, Wolters teaches that x is 0.80 to 0.85 (see rejection of claim 23 above). Wolters does not teach that x is about 0.90 to about 0.98. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wolters by having x being about 0.90 to about 0.98, since

it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 25 and 49, Wolters teaches substantially all the structure set forth in the claimed invention except x being about 0.95. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wolters by having x being about 0.95, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
May 12, 2005

Tom Thomas

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SUPERVISORY PATENT EXAMINER

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